REMARKS

This Amendment is responsive to the Official Action mailed on March 10, 2005, and for which a three-month extension is hereby requested.

MultiMediaCard Specifications

Concerning paragraph 2 of the Office Action, this requests that versions 1.0, 1.1, 1.2, and 1.3 of the MultiMediaCard System Specification be supplied. It is again noted that these are confidential, internal development documents. They do not constitute prior art under the provisions of 35 U.S.C. sections 102 and 103. These were not publicly available documents at the time of the application. It is currently being determined whether, under the provisions of their confidentiality agreements, they can be made public and submitted at this time; if so, they will be supplied. In any case, however, it is again noted that these documents are not applicable as prior art in the present application.

Title

The title of the invention has been amended along the lines suggested in the Office Action.

Objection to Claim 33

The Office Action objected to claim 33 on the grounds that it was not described in the application. This is respectfully submitted to be in error. Claim 33 contains the limitation of "wherein in response to too few tags being set, a received erase command is aborted." This is described on page 52 of the application at lines 9 and 10: "If there are too many untagged sectors/groups, the erase command is abort[ed]".

PRIOR ART REJECTIONS

The Office Action rejected claims 24-27 and 34-38 under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (U.S. patent number 5,509,134) or Harari et al. (U.S. patent number 5,418,752); rejected claims 24-27 and 34-36 as being unpatentable over Fandrich or Harari in view of Kishi et al. (U.S. patent number 4,841,432) or Noel et al. (U.S. patent publication 2002/00168891); rejected claims 18, 19, 22, 28-31, and 33 under 35 U.S.C. 103(a) as being unpatentable over Harari in view of Kaki et al. (U.S. patent number 5,809,515); and rejected claims 18-20 and 31 under 35 U.S.C. 103(a) as being unpatentable over Harari in

view of Kaki and further in view of Kishi or Noel. For the reasons given below, it is respectfully submitted that these various rejections of the pending claims are in error and should be withdrawn, as is disclosed below under the appropriate heading.

Claims 17, 21, 22, and 32 have been cancelled. Claim 18 has been rewritten in independent form and claims 22, 28, and 33 have had their dependence changed. The language of claim 22 has also be cleaned up. Additionally, as is also discussed below, new claims 39-41 have been added.

Rejection of Independent Claims 24, 25, and 37 based on Harari

The Office Action rejected independent claims 24, 25, and 37 under 35 U.S.C. 102(b) as being anticipated by Harari et al. (U.S. patent number 5,418,752).

First, it is noted that independent claims 24 and 25 incorporated the limitations of now cancelled independent claim 23 when they were rewritten in independent form in the Amendment mailed on May 27, 2004, in response to the Office Action mailed on February 27, 2004. The Office Action of February 27, 2004, (and that of September 18, 2003) only founds grounds for rejecting claims 24 and 25 under 35 U.S.C. 103(a) with Harari as the primary reference. In the Office Action of August 24, 2004, these rejections were removed. ***Consequently, the present Office Action contains rejections that have previously been made (the Office Action mailed on February 27, 2004) and overcome (by the arguments made in the Amendment mailed on May 27, 2004).*** Independent claim 37, which was not pending at that time, contains similarly limitations. It is unclear why the Office Action is re-including grounds for rejection which were not only incorrect but which have been previously withdrawn.

The arguments why these claims are not well founded is given in the following paragraphs, which it is believed make clear that a rejection of claims 24, 25, and 37 under 35 U.S.C. 102(b) as being anticipated by Harari is entirely without foundation. Reference is also made to the Amendments mailed on December 9, 2003, and May 27, 2004, where these arguments are developed in more detail.

Briefly, each of independent claims 24, 25, and 37 includes the limitations

> a plurality of group tags ... indicating whether the memory cells under the corresponding memory group are *write protected*;

where the emphasis has been added. Thus, these claims are drawn to *protecting* a group from writing. The Office Action cites column 6, lines 41-46, of Harari with respect to write

protection. As described in the cited location of Harari, the teachings of Harari are related to *enabling* an ***erase*** process:

> ...after all sectors intended for erase have been tagged, the controller *initiates an erase cycle to erase the group of tagged sectors.* ... [T]he controller shifts in a global command called Enable Erase into each Flash EEprom chip that is to perform an erase.

As the added emphasis shows, this process relates to erasing and the enabling of sectors for an ***erase*** process.

Thus, in distinction to Harari, claims 24, 25, and 37 are drawn to a *write* process, not an *erase*, and is about *protecting* groups of cells for this process, not *enabling* them. Harari provides no teachings related to write protection. Consequently, it is respectfully submitted that claims 24, 25, and 37 differ from the teachings of Harari in significant ways and that a rejection under U.S.C. 102(b) as being anticipated by Harari et al. (U.S. patent number 5,418,752) is not well founded and should be withdrawn.

Concerning claim 24, this also contains the limitation of "wherein the number of memory cells in each memory group is configurable". As already discussed, the teachings of Harari are directed are erase. What the Office Action appears to be taking as a "group" is the unit of erase in Harari, namely the sector. The number of cells in a sector is part of the physical structure of the array and is not configurable. (Similarly, the number of sectors in a an array is part of the physical structure of the array and is not configurable.) The locations in Harari cited by the Office Action all refer to flexibility in the selection of sectors and neither teach nor suggest that "the number of memory cells in each memory group is configurable", whatever the Office Action is identifying as a "group"---and, again, it is noted, this is all in reference to an erase process. Consequently, claim 24 is believed further allowable on this basis.

Concerning claim 25, this also contains the limitation of "wherein the corresponding cells in each memory group are calculated in real time". As already discussed, in the teachings of Harari, the number of cells in each sector (and the number of sectors in each array) is fixed. Consequently, there is nothing to calculate and a limitation such as "wherein the corresponding cells in each memory group are calculated" is lacking in Harari, whether it is calculated "in real time" or otherwise.

As to the locations in Harari cited by the Office Action, these all refer to the selection of sectors for erase and neither teach nor suggest that "the corresponding cells in each memory

group are calculated in real time". Consequently, claim 25 is believed further allowable on this basis.

As for claim 37, this also contains the limitation that "said group tags are settable in response to a command from a host to which the memory system is connected." The Office Action refers to Figure 3A, element 225. Element 225 is a command register; however, there is no disclosure of its being used for settable group tags set by the host (for write protection or for erase). Consequently, claim 37 is believed further allowable on this basis.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claims 24, 25, and 37 and their dependent claims (claims 26, 27, 34-36, and 38) under 35 U.S.C. 102(b) as being anticipated by Harari is not well-founded and should be withdrawn.

Rejection of Dependent Claims 34-36 and 38 based on Harari

The Office Action also rejected dependent claims 34-36 and 38 under 35 U.S.C. 102(b) as being anticipated by Harari. These claims are already believed allowable as their underlying independent claims are allowable for the reasons given above. They are also believed further allowable for their additional limitations.

Specifically, these claims all contain the limitation that the group tags are either settable or deselected by a host to which the card is connected. The Office Action refers to column 5, lines 25+, column 7, lines 13-19, and Figure 3A, element 225, of Harari; however, as is clear from column 5, lines 31-33, these operations are in response to the controller:

> The selection and subsequent erase operation are performed *under the control of the controller* **31**(see FIG. 2).

As is clear from the added emphasis, these tags are selected and deselected by the controller. And as is clear from Harari's Figure 1, the controller 31 is part of the card system 29, ***not*** part of the host. Harari neither teaches nor suggests that these tags be set or deselected by the host, but instead leaves these details to the controller on the card. It is again also noted that this all concerns *erase* operations, **not** write protection.

Consequently, dependent claims 34-36 and 38 are believed further allowable for these reasons.

Rejection of Independent Claim 24 based on Fandrich

The Office Action rejected independent claim 24 under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (U.S. patent number 5,509,134). This is respectfully submitted

to be incorrect. In particular, it is noted that ***previous Office Actions have themselves explicitly stated that Fandrich does not disclose all of the limitations of claim 24.*** Specifically, referring to lines 2-4 on page 3 of the previous Office Action (mailed on August 24, 2004), this states: "Fandrich does not specifically disclose the number of memory cells in each memory is configurable." It is respectfully submitted that, on this particular point, the previous Office Actions were correct and that the present Office Action is in error.

More specifically, with respect to the limitations of claim 24 the Office Action refers to the discussion of column 11, lines 28-36, of Fandrich, identifying the "groups" of the claim with the "blocks" of Fandrich. However, the "block" of Fandrich is the basic physical unit of erase of the flash memory. The number of cells in an erase block is part of the physical structure of the array and is not configurable. (In the particular embodiment disclosed by Fandrich at column 3, lines 55-60, the number of cells in a block corresponds to 64k bytes and the number of erase blocks per flash array is 32.) Consequently, not only is the number of memory cells in each block ***not*** configurable, but the limitation of "wherein the number of memory cells in each memory group is configurable" is, rather, contrary to the teachings of Fandrich.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 24 and its dependent claims (claims 26 and 34-36) under 35 U.S.C. 102(b) as being anticipated by Fandrich is not well-founded and should be withdrawn.

Rejection of Independent Claim 25 based on Fandrich

The Office Action also rejected independent claim 25 under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (U.S. patent number 5,509,134). This is respectfully submitted to be incorrect. In particular, as with clam it is noted that previous Office Actions have found that Fandrich does not disclose all of the limitations of claim 25, instead requiring secondary references to reject claim 25 under 35 U.S.C. 103(a). It is respectfully submitted that, on this particular point, the previous Office Actions were correct and that the present Office Action is in error.

More specifically, claim 25 contains the limitation of "wherein the corresponding cells in each memory group are calculated in real time". As already discussed, in the teachings of Fandrich, the number of cells in block, which the Office Action identifies with "memory group", (and the number of blocks in each array) is fixed. Consequently, there is nothing to calculate and a limitation such as "wherein the corresponding cells in each memory group are

calculated" is lacking in Fandrich. In particular, the Office Action refers to column 11, lines 29-36, for this limitation. This passage only refers to the setting of "lock bits" and has no disclosure of calculating the corresponding cells in a block and, in particular, has no disclosure of calculating this, or anything else, "in real time".

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 25 and its dependent claim (claim 27) under 35 U.S.C. 102(b) as being anticipated by Fandrich is not well-founded and should be withdrawn.

Rejection of Independent Claim 37 based on Fandrich

The Office Action also rejected independent claim 37 under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (U.S. patent number 5,509,134). This is respectfully submitted to be incorrect.

Claim 37 contains the limitation that "said group tags are settable in response to a command from a host to which the memory system is connected." Concerning the setting of group tags, the Office Action refers to column 11, lines 29-38, of Fandrich, identifying the "group tags" of the claims with the "lock bits" described there. As is clear from column 11, lines 29-38, of Fandrich, the lock bits are in the block status registers (BRSs); however, as is clear from column 7, lines 17-22, these operations are in response to the controller:

> ...The flash array controller **50** maintains status bits in the block status registers ...

As is clear from Fandrich's Figure 2, the flash array controller 50 is part of the card system 310, ***not*** part of the host. As far as can be determined, Fandrich neither teaches nor suggests that these tags be set "in response to a command from a host to which the memory system is connected", but instead leaves these details to the controller on the card.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 37 and its dependent claim (claim 38) under 35 U.S.C. 102(b) as being anticipated by Fandrich is not well-founded and should be withdrawn.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claims 24, 25, and 37 and their dependent claims (claims 26, 27, 34-36, and 38) under 35 U.S.C. 102(b) as being anticipated by Fandrich is not well-founded and should be withdrawn.

Rejection of Dependent Claims 34-36 and 38 based on Fandrich

The Office Action also rejected dependent claims 34-36 and 38 under 35 U.S.C. 102(b) as being anticipated by Fandrich. These claims are already believed allowable as their underlying independent claims are allowable for the reasons given above. They are also believed further allowable for their additional limitations.

Specifically, these claims all contain the limitation that the group tags are either settable or deselected by a host to which the card is connected. The Office Action refers to column 11, lines 29-38, of Fandrich, identifying the "group tags" of the claims with the "lock bits" described there. As is clear from column 11, lines 29-38, of Fandrich, the lock bits are in the block status registers (BRSs); however, as is clear from column 7, lines 17-22, these operations are in response to the controller:

> ...The flash array controller **50** maintains status bits in the block status registers ...

As is clear from Fandrich's Figure 2, the flash array controller 50 is part of the card system 310, ***not*** part of the host. As far as can be determined, Fandrich neither teaches nor suggests that these tags be set or deselected "in response to a command from a host to which the memory system is connected", but instead leaves these details to the controller on the card.

Consequently, dependent claims 34-36 and 38 are believed further allowable for these reasons.

Rejection of Independent Claims 24 and 25 based on Harari or Fandrich in view of Kishi

The Office Action also rejected independent claims 24 and 25 as being unpatentable over Fandrich or Harari in view of Kishi et al. (U.S. patent number 4,841,432). This is respectfully submitted to be incorrect.

(The Office Action does not actually refer to Harari in any of the rejections in this section (paragraph 7) of the Office Action. Consequently, it is unclear on what basis these Harari-based rejections are being made. If Harari is being combined with Kishi or Noel for the same reason as is done for Fandrich, then the following arguments also apply to the Harari-based rejections. For more detail, see the discussion of the rejection of claim 18 over Harari in view of Kaki and further in view of Kishi or Noel given below.)

More specifically, with respect to the limitations of claim 24 the Office Action refers to the discussion of column 11, lines 28-36, of Fandrich, identifying the "groups" of the claim with the "blocks" of Fandrich. However, the "block" of Fandrich is the basic physical unit of erase of the flash memory. The number of cells in an erase block is fixed, as it is determined by the physical structure of the array. (In the particular embodiment disclosed by Fandrich at

column 3, lines 55-60, the number of cells in a block corresponds to 64k bytes and the number of erase blocks per flash array is 32.) Consequently, as all ready noted, not only is the number of memory cells in each block not configurable, but the limitation of "wherein the number of memory cells in each memory group is configurable" is, rather, contrary to the teachings of Fandrich.

Thus, according to the teachings of Fandrich, each of its "lock bits" is explicitly tied to an erase block; an erase block of a flash memory is determined by its physical structure so that each cell is assigned to a specific, fixed block and cells can not be shifted between blocks; consequently, the number of memory cells in a given block is fixed and cannot be configured and such a configuring of the number of memory cells in each block (which the Office Action identifies with the "group" of the claim) is contrary to the teachings of Fandrich.

(As for Harari, as already discussed, in the teachings of Harari, the number of cells in each sector and the number of sectors in each array is fixed as part of the physical structure of the flash memory; consequently, an argument similar to that given for Fandrich applies and is given below with respect to claim 18.)

The Office Action cites Kishi for the limitation of "wherein the number of memory cells in each memory group is configurable". This is believed to be incorrect for a number of reasons. A first of these is that the Kishi patent is entirely directed at the reconfiguration of *tapes* for controlling machine tools and the methods described there are only compatible with a memory medium of a continuous nature, such as a magnetic tape, and are not compatible with a memory formed of discreet memory cells physically formed into fixed composite structures, such as the block of Fandrich. The teachings of Kishi requires that boundaries of a storage area can be incrementally moved in continuous manner, something that is possible on a medium such as data stored on a tape, but which is not possible for a memory formed of discreet memory cells physically formed into fixed composite structures of multiple cells.

Another reason why this is believed in error is that what Kishi is reconfiguring is not what is in a storage area itself, but rather is directed at reducing the unused blank portion of the tape between such storage areas. This can be seen from Figure 3 of Kishi, which is also the cover figure there. Such a shifting of empty space between erase blocks is not something that can be done in the context of a flash memory formed of fixed erase blocks.

Further, as discussed in more detail in previous responses, the teachings of Kishi are not readily combinable with those of Fandrich. The Office Action states in lines 17 and 18, page 9 that "the number of memory cells in each memory group is configurable as shown in

Kishi". This is incorrect and Kishi shows no such thing: Kishi has no disclosure of memory cells as the Kishi patent is entirely directed at the reconfiguration of *tapes* for controlling machine tools.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 24 and its dependent claims (claims 26 and 34-36) under as being unpatentable under 35 U.S.C. 103(a) as being over Fandrich in view of Kishi is not well-founded and should be withdrawn.

Concerning claim 25, claim 25 contains the limitation of "wherein the corresponding cells in each memory group are calculated in real time". As already discussed, in the teachings of Fandrich, the number of cells in block, which the Office Action identifies with "memory group", (and the number of blocks in each array) is fixed. Consequently, there is nothing to calculate and a limitation such as "wherein the corresponding cells in each memory group are calculated" makes no sense. With respect to claim 25, the Office Action states "Kishi further discloses the corresponding cells in each memory sector is calculated in real time (col.5 lines 32-42)." The sort of area reconfiguration Kishi describes in this passage again relates to the re-allotment of blank space, not calculating "the corresponding cells in each memory group". As already noted, Kishi is dealing with a very different technology that would not be obvious to combine with the other reference and which is not based on the cells found in the claims. Consequently, whatever Kishi is up to in the cited location (column 5, lines 32-42), it is not calculating "number of memory cells in each memory sector".

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 25 and its dependent claim (claim 27) as being unpatentable under 35 U.S.C. 103(a) as being over Fandrich in view of Kishi is not well-founded and should be withdrawn.

Rejection of Independent Claims 24 and 25 based on Harari or Fandrich in view of Noel

The Office Action also rejected independent claims 24 and 25 as being unpatentable over Fandrich or Harari in view of Noel et al. (U.S. patent publication 2002/00168891).

(As noted above, the Office Action does not actually refer to Harari in any of the rejections in this section (paragraph 7) of the Office Action. Consequently, it is unclear on what basis these Harari-based rejections are being made. If Harari is being combined with Kishi or Noel for the same reason as is done for Fandrich, then the following arguments also

apply to the Harari-based rejections. For more detail, see the discussion of the rejection of claim 18 over Harari in view of Kaki and further in view of Kishi or Noel given below.)

Considering the alternate rejections (or further rejections) based on Noel, with respect to claim 24, the Office Action states that "Noel discloses the number of memory cells in each memory sector is configurable (block 265) for the purpose of optimizing configuration of the memory." It is respectfully submitted that both of these statements are incorrect.

The Noel application is directed at multiprocessor computer architectures in which processors and other computer hardware resources are grouped into partitions. Specifically, it divides a single physical machine into separate logical partitions to act as independent processors. The cited location (block 256) is related to a software configuration and mentions memory only to describe the relative privileges that the various logical partitions have to the processors' memory. It is unclear how these teachings can be applied to the limitation of "wherein the number of memory cells in each memory group is configurable", as there is nothing corresponding to either "memory cells" or "memory group" into which they are formed and which could be reconfigured, which, as has already been noted, is contrary to the teachings of Fandrich.

Noel is instead concerned with a very different set of problems and technologies. In particular, there appears to be no disclosure of a memory system where "the number of memory cells in each memory sector is configurable"---or, for that matter, even the use of memory cells themselves in the teachings of Noel, as it is concerned with the logical partitions of a machine into independent processors.

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 24 and its dependent claims (claims 26 and 34-36) under as being unpatentable under 35 U.S.C. 103(a) as being over Fandrich in view of Kishi is not well-founded and should be withdrawn. It is believed neither obvious to combine Noel with the other references nor how to do so as the concerns of Noel a very different subject related to multiprocessor computer architectures and having nothing to do with memories based on cells and sectors found in the claims.

Concerning claim 25, claim 25 contains the limitation of "wherein the corresponding cells in each memory group are calculated in real time". As already discussed, in the teachings of Fandrich, the number of cells in block, which the Office Action identifies with "memory group", (and the number of blocks in each array) is fixed. Consequently, there is nothing to calculate and a limitation such as "wherein the corresponding cells in each memory group are

calculated" makes no sense. With respect to claim 25, the Office Action states "Noel further discloses the corresponding cells in each memory sector is calculated in real time (block 256, software configuration reads on this limitation, since it runs in real time)." First, a "software configuration" is entirely different from calculating "wherein the corresponding cells in each memory group". Secondly, the software running is itself not the same thing as it being configured.

As already noted, Noel is dealing with a very different technology, namely software, that would not be obvious to combine with Fandrich and which is not concerned with cells and sectors as found in the claims. Consequently, whatever Noel is up to in the cited location (block 256), it is neither calculating "number of memory cells in each memory sector" nor "the corresponding sectors in each memory group". Additionally, Noel states that "it is possible to dynamically change partitions", but gives no description of doing this "in real time".

For any of these reasons, it is respectfully submitted that the Office Action's rejection of independent claim 25 and its dependent claim (claim 27) as being unpatentable under 35 U.S.C. 103(a) as being over Fandrich in view of Noel is not well-founded and should be withdrawn.

Rejection of Dependent Claims 34-36 based on Harari or Fandrich in view of Kishi or Noel

The Office Action also rejected dependent claims 34-36 as being unpatentable over Fandrich or Harari in view of Kishi or Noel. These claims are already believed allowable as their underlying independent claims are allowable for the reasons given above. They are also believed further allowable for their additional limitations. The basis given in the Office Action for these rejections is based on Fandrich and is the same as discussed above. Consequently, they are believed further allowable for the reasons given above under the "Rejection of Dependent Claims 34-36 and 38 based on Fandrich" heading.

Rejection of Independent Claim 18 based on Harari in view of Kaki

The Office Action rejected independent claim 18 and its dependent claims (19, 22, 28-31, and 33) under 35 U.S.C. 103(a) as being unpatentable over Harari in view of Kaki et al. (U.S. patent number 5,809,515). This is respectfully submitted to be incorrect.

(Claim 17 has been cancelled and claim 18 rewritten in independent form to more clearly delineate the distinctions over the prior art. Claims 22, 28, and 33 have had their

dependence changed from claim 17 to claim 18, and the language of claim 22 has also be amended to read better.)

Claim 18 contains the limitation of "wherein the number of memory sectors in each memory group is configurable". The Office Action refers to column 5, lines 25+, and column 7, lines 13-19. As discussed above, in Harari the number of cells in a sector is part of the fixed, physical structure of the array and is not configurable. Similarly, the number of sectors in an array is part of the fixed, physical structure of the array and is not configurable. The locations in Harari cited by the Office Action all refer to flexibility in the selection of sectors and neither teach nor suggest that "the number of memory sectors in each memory group is configurable", whatever the Office Action is identifying as a "group".

Concerning the final limitation of claim 18, this reads:

> wherein *any combination of memory sectors* in a memory group be *simultaneously erased, and any combination of the memory groups* can be *simultaneously erased.*

The emphasis has been added. The Office Action relies upon Kaki to supply these emphasized elements. This is believed to be in error and it is respectfully submitted that the teaching of Kaki are directly contrary to what is found in claim 18.

Rather than teaching that "any combination of memory sectors" and "any combination of the memory groups can be simultaneously erased", the teachings of Kaki are restrictive as to the combinations of erase units that can be set for erasing together. As described at column 7, lines 41-42, "areas to-be-erased are set *so as to be in different memory chips* of the flash memories 4", where the emphasis has been added. Consequently, Kaki only allows for one unit of erase per chip to set for erase together, whether the appropriate "area to-be-erased" is a sector or a whole chip. Thus, Kaki teaches away from the limitation of allowing *any combination of memory sectors* and *any combination of the memory groups* to be erased simultaneously.

Further, Kaki specifies that the erase of the units of erase are erased *sequentially, not simultaneously.* This is shown in Figure 4 of Kaki and is based on the loop in step 45, as described at column 7, lines 49-50: "Subsequently, the processor 2 determines if the next area to-be-erased exists (step 45)." So that rather than simultaneously erasing all of the units of erase set for erase, Kaki teaches that a sequential process must be used. The Office Action refers to column 7, lines 28-30, of Kaki, which states "Thus, the plurality of flash memories 4 are erased in parallel." This sentence, beginning with "thus", clearly refers to preceding paragraph, which it ends. This paragraph clearly describes a process in which nits of erase are

erased *sequentially, not simultaneously*. There may be a parallelism in that erase operations may be going on concurrently in different ones of the flash memories 4 shown in Kaki's Figure 1, but this is not the same as "wherein any combination of memory sectors in a memory group be simultaneously erased, and any combination of the memory groups can be simultaneously erased." Once again, Kaki specifies that the erase of the units of erase in a given memory are erased *sequentially, not simultaneously* and again teaches away from the limitations of the claim.

Concerning the use of two levels of tags, the group tags and the sector tags, the cited portion of Kaki states that the erase process described in the preceding discussion is changed according to erase structure used by flash memory; that is, it states that flash memories being used will have a specified unit of erase and that the techniques of the preceding paragraph have to conform with this unit of erase. In the preceding paragraph (beginning at column 7, line 32), this unit of erase is the sector, while in the cited portion (column 7, line 64, through column 8, line 14) the unit of erase is a whole chip. According to Kaki, what the Office Action identifies as "tags" correspond, and can only correspond, to specific unit of erase in the flash architecture. Kaki neither teaches nor suggests the use of two levels of tags for both the basic unit of erase (such as a sector) and the composite, multi-sector unit of the group. Instead, according Kaki, "tags" must correspond to the specific architecture's unit of erase: either sector tags, or rather what the Office Action is identifying as tags, or group tags, but not both.

For any of these reasons, it is believed that a rejection of claim 18 and its dependent claims (claims 19, 22, 28-31, and 33) under 35 U.S.C. 103(a) based on Harari in view of Kaki is not well founded and should be withdrawn. It is respectfully submitted that not only is it is not obvious to combine these two references in the manner recited in the claims, but that the Office Action is improperly combining the two references in a manner gained by hindsight of the present invention and in a manner that is explicitly contrary to the teachings of Kaki.

Rejection of Dependent Claims 19, 28-31, and 33 based on Harari in view of Kaki

The Office Action also rejected dependent claims 19, 28-31, and 33 under 35 U.S.C. 103(a) based on Harari in view of Kaki. These claims are already believed allowable as their underlying independent claim is allowable for the reasons given above. They are also believed further allowable for their additional limitations.

Concerning claim 19, this contains the additional limitation of "wherein the corresponding sectors in each memory group is calculated in real time." As discussed above, in Harari the number of sectors in an array is fixed; consequently, the number of sectors in each array (which, in the interpretation of the Office Action, correspond to the "group" of the claim) is not calculated at all. The portion of Harari cited in the Office Action rather corresponds to the *setting* of what is taken to correspond to the sector tags (the registers 221 of Harari's Figure 3A), not the *calculation of how many such registers exist, which is a* ***fixed number***. Further, Harari does not disclose this being done in "real time" as this is described in the present application.

Concerning claims 28-30, these claims all contain the limitation that the sector tags are either settable or deselected by a host to which the card is connected. The Office Action refers to column 5, lines 25+, column 6, lines 41-45, and Figure 1 of Harari; however, as is clear from column 5, lines 31-33, these operations are in response to the controller:

> The selection and subsequent erase operation are performed *under the control of the controller* **31**(see FIG. 2).

As is clear from the added emphasis, these tags are selected and deselected by the controller. And as is clear from Harari's Figure 1, the controller 31 is part of the card system 29, ***not*** part of the host. Harari neither teaches nor suggests that these tags be set or deselected by the host, but instead leaves these details to the controller on the card.

For claims 28-30, the Office Action also cites Kaki for the limitation that the group tags are either settable or deselected by a host to which the card is connected, referring to Kaki's Figure 4, references numbers 42-47. However, as is clear at column 7, lines 37-39, this is not done by the host but rather by the processor 2 (Figure 1), which, as is clear from Kaki's Figure 1, is part of the ***card, not the host***: "the processor 2 sets the physical sector Nos. of the flash memories 4 to-be-erased".

Concerning claim 31, this contains the additional limitation of "wherein the number of memory sectors in each memory group is configurable by a host to which the memory system is connected." As discussed above, in Harari the number of sectors in an array is fixed; consequently, the number of sectors in each array (which, in the interpretation of the Office Action, correspond to the "group" of the claim) is not configurable. The portion of Harari cited in the Office Action again instead corresponds to the *setting* of what is taken to correspond to the sector tags; further, as with claims 28-30, this process is not performed by the host, but by the on card controller. The Office Action refers to column 5, lines 25+,

column 7, lines 13-19, and Figure 1 of Harari; however, as is clear from column 5, lines 31-33, these operations are in response to the controller:

> The selection and subsequent erase operation are performed *under the control of the controller* **31**(see FIG. 2).

As is clear from the added emphasis, these tags are selected and deselected by the controller. And as is clear from Harari's Figure 1, the controller 31 is part of the card system 29, ***not*** part of the host.

As for claim 33, this contains the additional limitation of "wherein in response to too few tags being set, a received erase command is aborted." The cited portions of Harari refer to the ability to selective set or not set the registers for specific sectors and also to remove or skip specific sectors. This is quite different from aborting the whole erase command; it is also not is response to too few registers being set. The Office Action states that "not setting any sectors reads on" the limitation of "wherein in response to too few tags being set, a received erase command is aborted", but these are two quite distinct things.

Consequently, dependent claims 19, 28-31, and 33 are believed further allowable for any of these reasons.

Rejection of Independent Claim 18, 19, 22, and 31 based on Harari in view of Kaki further in view of Kishi or Noel

The Office Action rejected independent claim 18 and dependent claims 19, 22, and 31 under 35 U.S.C. 103(a) as being unpatentable over Harari in view of Kaki further in view of Kishi or Noel. This is respectfully submitted to be incorrect.

Concerning claim 18, the Office Action is again relying upon Kishi or Noel to provide the configurability not found in Harari or Kaki, either alone or combined. This is the same purpose for which the Kishi or Noel was invoked for claim 24, as described above. Consequently, this rejection is believed to be in error for all of the reasons given above with respect claim 24 concerning this issue. The Examiner is referred to the above discussion, which applies here, but will not be repeated as this is already a lengthy response.

Similarly, the Office Action also cites Kishi and Noel for the further limitations of dependent claims 19 and 31. As for claim 19, this recites limitations similar to those found in claim 25. Consequently, this rejection is believed to be in error for all of the reasons given above with respect claim 25 concerning this issue based on these references. The Examiner is

referred to the above discussion, which applies here, but will not be repeated as this is already a lengthy response.

As for claim 31, paragraph [0265] of Noel is about configuration of memories on a multiprocessor system, not about a host configuring an attached memory.

For any of these reasons, it is believed that a rejection of claim 18, 19, 22, and 31 under 35 U.S.C. 103(a) as being unpatentable over Harari in view of Kaki further in view of Kishi or Noel is not well founded and should be withdrawn.

New Claims

New claims 39-41 have been added. Similarly to the subject matter treated in claim 18 and its dependent claims, these claims are drawn to aspects of the erase tagging hierarch described beginning on page 49, line 15, of the present application and are believed allowable for many of the reasons given above.

Conclusion

Therefore, for any of the above reasons it is respectfully submitted that a rejection of claims 18, 19, 22, 24-31, and 33-38 under the stated reasons is not well founded and should be withdrawn. Reconsideration of claims 18, 19, 22, 24-31, and 33-38, along with consideration of new claims 39-41, and an early indication of their allowance are respectfully requested.

Respectfully submitted,

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